



## Improving Output Voltage Ripple of the NCP3063 Series of Switching Regulators by Applying a Simple Feedforward Technique

Prepared by: Dennis Solley  
ON Semiconductor

The NCP3063 Switching Regulator is an improved version of the popular MC34063 switching regulators and is based on a very flexible hysteretic architecture that can be used to create step-down (buck), step-up (boost) and buck-boost voltage regulators. This device can support input and output voltages up to 40 V<sub>DC</sub> which makes it attractive for a wide array of switching regulator applications, be it boosting a 5 V rail up to 24 V or stepping down a 12 V supply to 5 V or dealing with a wide input

voltage from a Lead-Acid battery. The techniques discussed in this application note will assist the designer in optimizing their design to the specific V<sub>IN</sub> and V<sub>OUT</sub> requirements of their application and allowing them to improve output ripple performance when they do not require operating the DC-DC converter near the maximum duty cycle of the NCP3063.

The block diagram of the NCP3063 controller is shown in Figure 1.

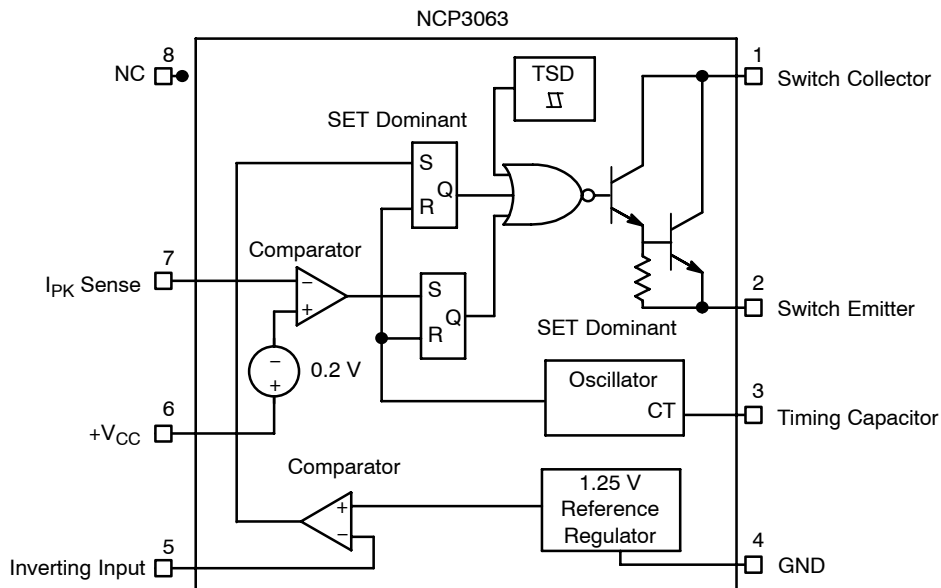
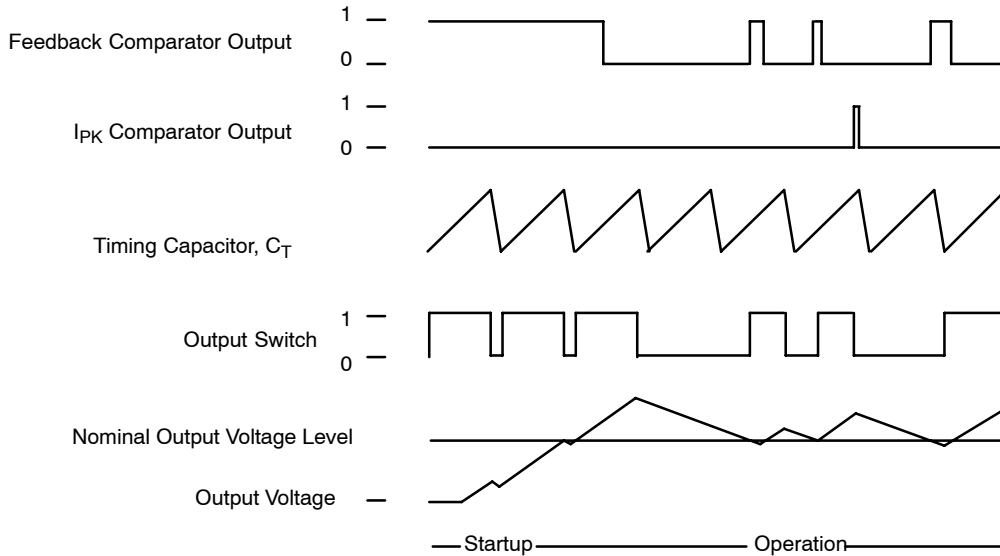


Figure 1. Block Diagram of NCP3063

## AND8284/D

The oscillator section consists of two current sources; one charging, the other discharging the timing capacitor  $C_T$ , between two fixed voltage levels. The levels are approximately 500 mV apart. The ratio between the charge

current and the discharge current is set within the controller to be 1:6. This ratio creates a fixed duty cycle  $D_{MAX}$  of 6/7 or 0.86. Typical operating waveforms, including the timing ramp  $C_T$ , are illustrated in Figure 2.



**Figure 2. Typical Operating Waveform**

This versatile controller can be configured for buck, boost, buck-boost and also inverting applications. For detailed information regarding controller operation refer to the NCP3063 data sheet. The essentials of the control method can be observed in the waveforms of Figure 2. The output voltage is fed back to the inverting input (Pin 5) of the comparator (Figure 1) via a resistor divider. If the output is above or below the setpoint, the comparator “gates” a series of clock cycles through the power switch. Control of the output voltage is achieved by varying the average number of “on cycles” to the number of “off cycles” in a given time interval.

The transfer functions (or gain)  $V_{OUT}/V_{IN}$  for buck, boost and buck-boost operation, neglecting circuit losses, are given by the following equations:

$$\text{Buck Transfer Function} = D \quad (\text{eq. 1})$$

$$\text{Boost Transfer Function} = \frac{1}{(1 - D)} \quad (\text{eq. 2})$$

$$\text{Buck-Boost Transfer Function} = \frac{D}{(1 - D)} \quad (\text{eq. 3})$$

If the value  $D_{MAX}$  equal to 0.86 is inserted into the above equations, the maximum gain available for each topology is determined.

Maximum buck gain = 0.86

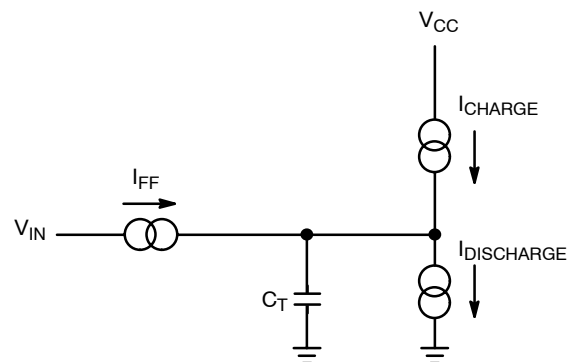
Maximum boost gain = 7.14

Maximum buck-boost gain = 6.14

The maximum gain values indicated above may be considerably more than a particular application requires. For example a 12 V to 5 V buck application requires a gain of

0.42 and a corresponding  $D = 0.42$ , a 12 V to 19 V boost application requires a gain of 1.58 resulting in a nominal  $D = 0.37$ , while a 12 V to 12 V buck-boost application requires unity gain and  $D = 0.5$ . Hence dependent on the application, the ratio of “on pulses” to “off pulses” can be very large or very small, to maintain output regulation against a given set point. In turn, this may result increased output ripple, requiring a large output capacitor. In extreme cases, audible noise generation is possible, if the pulse repetition rate is in the audio band.

The addition of a feedforward resistor can help to alleviate these issues. The ramp circuit is modified as illustrated in Figure 3 by the addition of an external current source  $I_{FF}$  at the  $C_T$  pin. This current source, in the simplest case, is created by adding a resistor between  $V_{IN}$  and  $C_T$ .



**Figure 3.**

## AND8284/D

Adding an external current will reduce the time it takes to charge the  $C_T$  capacitor between the ramp's minimum and maximum thresholds. The design equations relating to the oscillator section are given below.

$$T_{ON} = C_T * V_{RAMP} / \sum I_{CHARGE} \quad (\text{eq. 4})$$

$$T_{OFF} = C_T * V_{RAMP} / \sum I_{DISCHARGE} \quad (\text{eq. 5})$$

$$T_S = (T_{ON} + T_{OFF}) \quad (\text{eq. 6})$$

$$D_{MOD} = \frac{T_{ON}}{T_{OFF}} \quad (\text{eq. 7})$$

$$F_S = \frac{1}{T_S} \quad (\text{eq. 8})$$

Table 1 shows the corresponding reduction in duty cycle  $D_{MOD}$  as a normalized function of the charging and discharging currents flowing into the timing capacitor  $C_T$ . The table also shows the change in normalized oscillator frequency.

Once an optimum duty cycle has been identified and  $I_{FF}$  selected, the value of  $C_T$  can be ratio metrically adjusted to set the design frequency. Once set, the frequency variation against duty cycle is small over a wide range of external charging currents.

**Table 1. VARIATION OF DUTY CYCLE  $D_{MOD}$  AND FREQUENCY  $F_{MOD}$  AS A FUNCTION OF NORMALIZED EXTERNAL CURRENT, CHARGING THE TIMING CAPACITOR  $C_T$ .**

External Charging Current	Internal Charging Current	Internal Discharging Current	Duty Cycle $D_{MOD}$	Frequency $F_{MOD}$
0	1	6	0.86	1.00
1	1	5	0.71	1.43
2	1	4	0.66	1.71
3	1	3	0.50	1.71
4	1	2	0.29	1.43
5	1	1	0.14	0.86

Practical Example

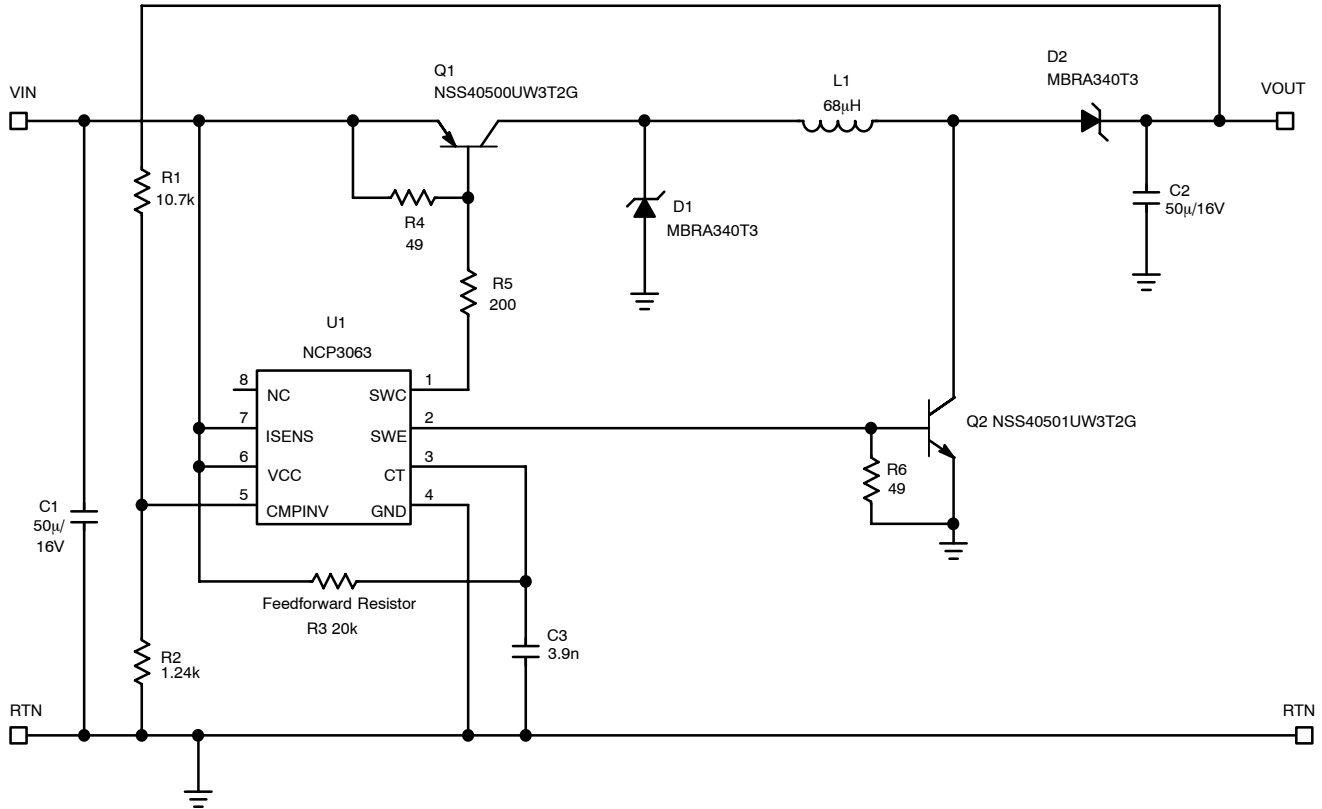


Figure 4. Schematic of a Noninverting Buck-Boost Topology

Figure 4 is a schematic of a noninverting buck-boost topology. The input is a nominal 12  $V_{IN}$  while the output is regulated to 12  $V_{OUT}$ . Assuming no circuit losses, the transfer function or gain of this application is unity and the duty cycle determined from the buck boost transfer function is 0.5. Referring to Table 1, a 3:1 ratio for the external charging current to internal charging current would generate a modified duty  $D_{MOD}$  of 0.5.

However, to accommodate conduction and switching losses in the power components, we will start by selecting a 2:1 ratio, providing a  $D_{MOD}$  of 0.66 and modified gain (Equation 3) of 0.66/0.34 or 1.94.

The nominal charge and discharge currents for the NCP3063 are listed below:

- Charging Current is 260  $\mu A$  @ 5 V  $V_{CC}$  / 25°C and 280  $\mu A$  @ 40 V  $V_{CC}$  / 25°C.
- Discharging Current is 1550  $\mu A$  @ 5 V  $V_{CC}$  / 25°C and 1700  $\mu A$  @ 40 V  $V_{CC}$  / 25°C.

The data above may be verified from measurements of the  $C_T$  ramp illustrated in Figure 5 before inserting the feedforward resistor R3 in Figure 4.

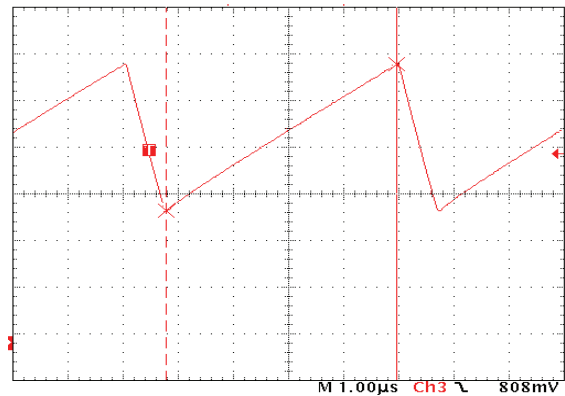


Figure 5. Ramp Waveform  
 $C_T = 1800$  pF,  $T_S = 4.94$   $\mu S$

Rearranging Equation 4, the charge current  $I_{CHARGE}$  is given by the expression

$$I_{CHARGE} = C_T * \Delta V_{RAMP} / T_{ON} \quad (eq. 9)$$

Substituting the measured values taken from the ramp waveform in Figure 5 into Equation 9,  $I_{CHARGE} = 1800 \text{ pF} * 628 \text{ mV} / 4.18 \text{ } \mu\text{s} = 270 \text{ } \mu\text{A}$  which corresponds to the data above.

For  $D_{MOD}$  of 0.66, we require an external current of  $520 \text{ } \mu\text{A}$ . The average ramp voltage from Figure 5 is  $0.9 \text{ V}$  and  $V_{IN}$  is nominally  $12 \text{ V}$ , hence the value of the feedforward resistor R3 may be determined from the expression  $(12 \text{ V} - 0.9 \text{ V}) / 520 \text{ } \mu\text{A}$  or  $21.3 \text{ k}\Omega$ . A preferred value of  $20 \text{ k}\Omega$  is selected;  $I_{FF}$  is then  $555 \text{ } \mu\text{A}$ .

$$\sum I_{CHARGE} = 555 \text{ } \mu\text{A} + 270 \text{ } \mu\text{A} = 0.825 \text{ mA}$$

$$\sum I_{DISCHARGE} = 1550 \text{ } \mu\text{A} - 555 \text{ } \mu\text{A} = 0.995 \text{ mA}$$

From Table 1, it is apparent that in order to maintain the same switching frequency  $F_S$  after an external current source is added in circuit, the value of the timing capacitor  $C_T$  has to be increased by a design factor 1.72 times. Here  $C_T$  was increased to  $3.9 \text{ nF}$ .

$$C_T * \Delta V_{RAMP} = 3.9 \text{ nF} * 560 \text{ mV} = 2.18 \cdot 10^{-9}$$

Substituting the values above into Equations 4 and 5 gives:

$$T_{ON} = 2.64 \text{ } \mu\text{s} \quad T_{OFF} = 2.19 \text{ } \mu\text{s}$$

$$T_S = (T_{ON} + T_{OFF}) = 4.83 \text{ } \mu\text{s}$$

$$D_{MOD} = \frac{T_{ON}}{T_S} = 0.547$$

$$F_S = \frac{1}{T_S} = 207 \text{ kHz}$$

The modified ramp is captured in Figure 6.

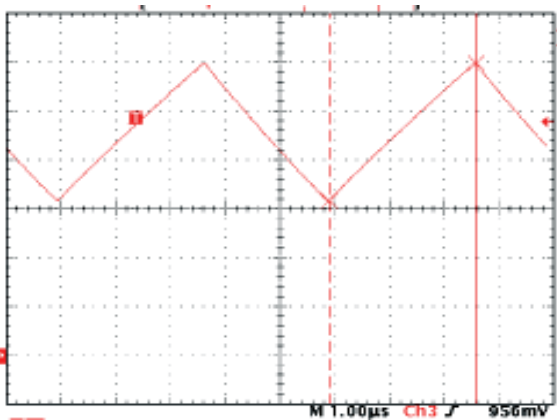


Figure 6. Modified Ramp Waveform,  $C_T = 3.9 \text{ nF}$ ,  $I_{FF} = 555 \text{ } \mu\text{A}$

Data measured from the ramp waveform in Figure 6 is given below and shows good correlation with the calculated results above.

$$T_{ON} = 2.68 \text{ } \mu\text{s} \quad T_{OFF} = 2.28 \text{ } \mu\text{s}$$

$$T_S = (T_{ON} + T_{OFF}) = 4.96 \text{ } \mu\text{s}$$

$$D_{MOD} = \frac{T_{ON}}{T_{OFF}} = 0.54$$

$$F_S = \frac{1}{T_S} = 202 \text{ kHz}$$

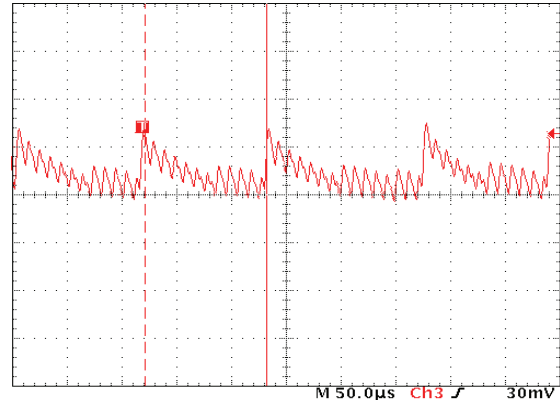


Figure 7. Buck-Boost Output Ripple with Voltage Feedforward Applied

The output ripple across a  $33 \text{ } \mu\text{F}$  electrolytic and  $20 \text{ } \mu\text{F}$  MLCC capacitors in parallel is shown in Figure 7. The output voltage is regulated at  $11.9 \text{ V}$ . The ripple is  $70 \text{ mV}$  peak to peak with a repetition rate around  $9 \text{ kHz}$ .

The collector waveform of the NPN transistor Q2 and modified  $C_T$  ramp are illustrated in Figure 8. It is observed that energy is flowing from primary to secondary for many switching cycles to support the  $100 \text{ mA}$  output load. The converter was then operated without feedforward at the same switching frequency. The output capacitor bank and the load were identical. The output ripple is shown in Figure 9.

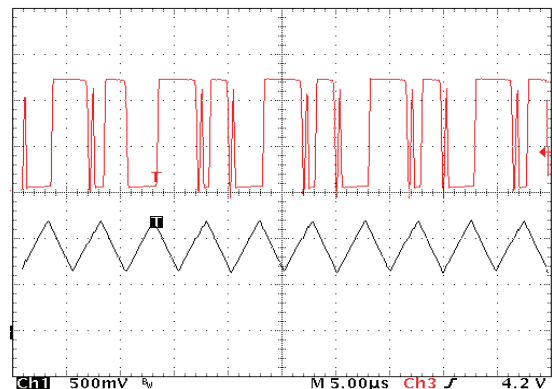
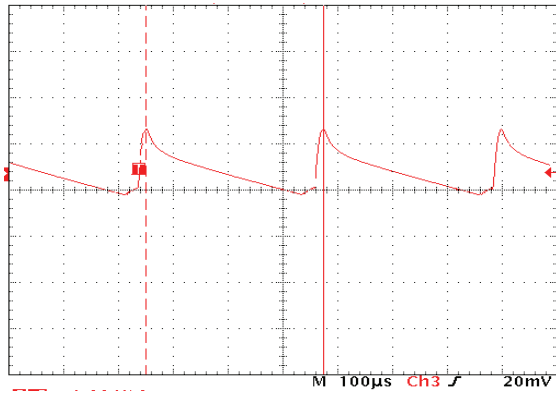
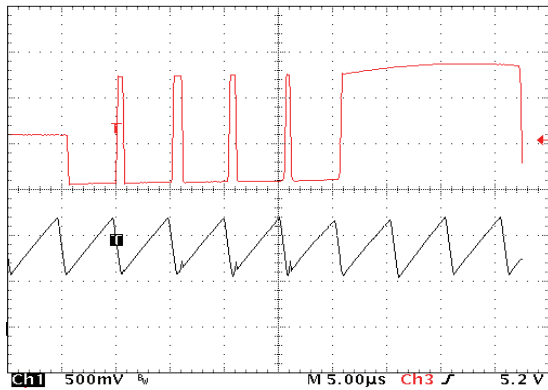


Figure 8. Collector Waveform Q2 with Modified Ramp  $D_{MOD}$



**Figure 9. Buck Boost Output Ripple Without Feedforward Applied**

It is evident that the output ripple has increased to 1.2 V peak-to-peak with a repetition rate around 3 kHz and the higher ripple of the output waveform results in the average output voltage being regulated at 12.3 V.




**Figure 10. Collector Waveform Q2 with  $D_{MAX}$  Ramp**

The collector waveform of the NPN transistor Q2 and  $D_{MAX}$  ramp is shown in Figure 10. Here it is evident that the energy flow to support the same 100 mA output is drawn from the input in five switching cycles, during which time the voltage on the output capacitor C2 is increased by 1.2 V. C2 is discharged by the output load for several hundred microseconds before the gate oscillator in the NCP3063 restarts.

**Conclusion**

By summing an external current source into the  $C_T$  pin of the NCP3063, it is possible to optimize the open loop gain of buck, boost or buck boost topologies for any given application. Reducing the controller’s maximum duty cycle of 0.86 to a lower value  $D_{MOD}$  allows the power components to be designed for lower stress. Input capacitors, output capacitors, inductor, switches and diodes can all benefit from the  $D_{MAX}$  reduction. The effect of output capacitor ripple was investigated in the particular case of a buck-boost topology. It is evident that a large reduction in output capacitor is possible when a single resistor feedforward function is implemented. This technique can also be applied to the MC33063/MC34063 but be aware that the ramp charge and discharge currents are different.

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. “Typical” parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT:**  
 Literature Distribution Center for ON Semiconductor  
 P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
 Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
 Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
 For additional information, please contact your local Sales Representative